Miguel Tirado

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Qualification Summary

- BS Computer Engineering
- Strong team, communication and organization skills developed through work experience, projects, and professional activities.
- 1 year of experience working on an interdisciplinary team throughout a full project development life cycle.
- Experienced use with FPGA's and Verilog through course work and projects.
- ***Languages:*** Java • C • Verilog • Python •VHDL • SQL • Assembly (x86 and MIPS) • HTML/CSS
- ***Hardware:*** FPGA (Xilinx Spartan 3E/DEO-NANO), Raspberry Pi, Arduino, Parallax Propeller Board,STM32, Oscilloscopes
- ***Tools:*** PSpice, Cadence Virtuoso, Wireshark, Synopsys, Quartus Altera II, Xilinx ISE Design Suite, PuTTY, Git, GitHub, Bitbucket, GNU Debugger, VM ware, MS office
- ***Systems:*** Linux/Unix, Windows, MacOS X
- Multilingual: English, Spanish

Education

BS, Computer Engineering • CSU, Sacramento • Overall GPA 3.72 | Major GPA: 3.74 • *December 2020*

Related Coursework:

UNIX System Programing	Programming Concepts and Methodology, I & II	Computer Hardware Design
Discrete Structures	Data Structures and Algorithm Analysis	Adv. Computer Organization
Operating System Principles	Advanced Logic Design	Signals and Systems
Network Analysis	Computer Interfacing	CMOS and VLSI Design
Electronics	Computer Networks & Internet	Probability & Random Signal
Database Mgmt. Systems	Operating Systems Pragmatic	Senior Design Project I & II

Projects

Senior Project Design – Pedestrian Safety Device *Spring/Falll 2020*

Member of a 4-person team that developed devices that will prevent the collisions of low-speed personal vehicles. The devices use a collision detection algorithm to use their location and velocity to calculate the time to collision from one device to the other. The devices communicate with each other by sending and receiving their location and velocity wirelessly through ESP-NOW. Personally, responsible for developing the communication aspect by using ESP-32's own communication protocol and developed a 150-line C communication program that was integrated with other features.

Simple Operating System *Fall 2020*

Member of a 3-person team that designed and implemented a simple process scheduling operating system by using a special development operating environment called SPEDE. The operating system ran on Intel's x86 CPU architecture where a MS DOS based environment was used for testing and Ubuntu Linux was used for development. These environments were run on a virtual machine due to the global pandemic. Topics covered and implemented in our operating system are the Kernel, Processes, and Interprocess Communication. The operating system used its own api and was programmed in C and inline assembly.

CMOS and VLSI Chip Layout Design *Spring 2020*

Designed 0.18um chips (NAND, Inverter, and Ring Oscillator) that use CMOS and VLSI concepts, methodologies, and techniques. The project had requirements such as midpoint voltage values, rise, and fall time values while following the design rules of the CMOS process. The chips were tested and validated by going through and DRC and LVS chip layout verification.

Computer Network Labs *Spring 2020*

Analyzed basic HTTP Get/response and condition Get/response interaction by using Wireshark packet sniffer. Also set up a simple web server using Python 3 that would host a simple HTML file. Created a python program that would print out server response when ran from my school server it then would proceed to send me an email. *Wireshark, Python 3*

Simplified Microprocessor Design, Verilog *Spring 2019*

Developed a simplified microprocessor that was made up of a data path and control path. The data path followed a schematic that was made up with multiplexers, D-Flip Flops, and a arithmetic logic unit while the control path was made up by a finite state machine. Behavioral and combinational modeling in Verilog were used along with a FPGA (Xilinx Spartan 3E) for testing purposes. ***Tools: Verilog, FPGA, Xilinx ISE Design Suite***

16-bit MIPS Processor, Verilog *Fall 2019*

Led a two-person team through the design, development, and implementation phases of a 16-bit microprocessor with a 5-stage pipeline. The processor specifications were based on the professor's criteria but followed MIPS format as a reference. Behavioral and combinational modeling in Verilog was used in the design of the processor's components.

Solar Tracker Project *Fall 2018*

Helped to lead a 3-person team through the design, development, and implementation of solar tracker that would send data through email by using Parallax microcontroller and raspberry pi 3. Personally, built the foundation and wrote a 50-line C script that would rotate the solar panel depending on light level from east to west.

Java & C Projects *Fall 2017*

- Developed a word count program with over 900 lines of code as a class final project with a team of 2. The user can obtain the number of words inside a txt file by frequency or by unique words and can choose the type of algorithm to perform the task. Responsible for developing AVL trees and binary search trees onto the program. *Java Program*
- Implemented a GUI checkbook system with 400 lines of code, where the user can create accounts, make deposits, withdraw cash, save and load their transactions and store in a file. *Java program*
- Designed a kernel module with 135 lines of code that would store a person's birthday inside a linked list and then sort the list by oldest to youngest. The module would also allocate and deallocate memory to save space. *C Program*
- Developed a mini shell with over 244 lines of code combined that handled Linux commands such as exit, pwd, or cd and handled redirection of files. *C Program*

Simple SQL Database Fall 2020

Formed a SQL database based on the relational and ER diagrams provided by the professor. Made sure to follow the constraints from the diagram and to populate the database for testing purposes. MySQL 5.6 was used when creating this database. *Tools: Putty, SQL*

1st place Sacramento Hackathon III Spring 2020

Member of a 4-person team that won best hardware project for developing a capacity assistant that would record the amount of people entering and leaving a building and then update a website in real time. The project was constrained to 36 hours and used a raspberry pi 3 to measure the amount of people and to host the website. Responsible for helping develop the website by using python CGI and Apache 2.

Experience

Embedded Systems Intern ***Network Sound, Sacramento*** *12/2019 – 3/2020*

Helped the company transition from FPGA use towards microcontrollers by developing C and Python scripts that would allow wireless capabilities and control towards new audio products. Developed programs that would allow UDP communication with the audio product and the user.

Director of Academics ***Society of Hispanic Professional Engineers*** *08/2019 – 05/2020*

Responsible for helping 40+ members achieve higher grades by promoting support services, conducting workshops, study sessions, and providing tutoring. Worked alongside a team of 12 student officers to improve and empower engineering students on campus.

Mentor ***MESA Professional Mentor Program*** *09/2018 – 05/2019*

Helped a student towards their first year in college by being a mentor and leader. Lead the student to pursue higher grades and extracurricular activities. Provided tutoring, guidance, and support through difficult courses.

Crew Member/Trainer ***McDonalds, Sacramento*** *8/2016 - Present*

Help train new crew members on safety, food handling, area maintenance, and effective teamwork increasing efficiency and resulting in faster and better customer service. Developed strong leadership, communication, team, organization skills and learned to take initiative.

Professional Activities

SHPE – Officer 1 year, member 4 years
MESA (Engineering Program) – Member 4 years
Tau Beta Pi (Engineering Honor Society) – Member 2 years
IEEE – Member 3 years

Awards & Accomplishments

HITEC Foundation Scholarship
Cien Amigo IME scholarship
CSUS ASI Scholarship
Deans Honor roll (4 years)